

AMENDMENTS

Please amend the claims as indicated hereafter.

1. (Currently Amended) An integrated circuit comprising:
 - a first port for outputting a signal;
 - a second port for receiving said signal;
 - a common area comprising an alignment link for electrically connecting said first port with said second port;
 - said first port is directly and electrically ~~connected~~ wired traced to said alignment link from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with said first port and said common area;
 - said second port is directly and electrically connected to said alignment link from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports with said second port and said common area; and
 - said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port; said alignment link is arranged within said common area.
2. (Currently Amended) An integrated circuit according to claim 1 wherein said alignment link further comprises ~~comprise~~ a wiring trace.
3. (Canceled)
4. (Previously Amended) An integrated circuit according to claim 1 wherein said first port is located in said first area of integrated circuit real estate.
5. (Previously Amended) An integrated circuit according to claim 1 wherein said second port is located in said second area of integrated circuit real estate.

6. (Currently Amended) An integrated circuit comprising:
 - a first port located in a first area of integrated circuit real estate, for outputting a signal;
 - a second port located in a second area of integrated circuit real estate, for receiving said signal;
 - a common area comprising an alignment link for electrically connecting said first port with said second port;
 - said first port is directly and electrically ~~connected~~ wired traced to said alignment link from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with said first port and said common area;
 - said second port is directly and electrically connected to said alignment link from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports with said second port and said common area;
 - said alignment link comprises a signal buffer for buffering a signal traveling along said alignment link between said first port and said second port; and
 - said integrated circuit real estate comprises multi-levels.

7. (Original) An integrated circuit according to claim 6 wherein said multi-levels comprise a semiconductor level and a wire tracing level.
8. (Original) An integrated circuit according to claim 7 wherein said semiconductor level comprises said signal buffer.
9. (Original) An integrated circuit according to claim 7 wherein said wire-tracing level comprises said first port and said second port.
10. (Previously Amended) An integrated circuit according to claim 9 wherein said wire-tracing level comprises a plurality of wire-tracing levels.

11-16 (Canceled)

17. (Currently Amended) An integrated circuit comprising:
a first port for outputting a signal;
a second port for receiving said signal;
a common area comprising an alignment means for electrically connecting said first port with said second port;

 said first port is directly and electrically connected wired traced to said alignment means from a first area without the use of a first linking area that includes bridging traces for linking mis-aligned ports with said first port and said common area; and

 said second port is directly and electrically connected to said alignment means from a second area without the use of a second linking area that includes bridging traces for linking mis-aligned ports with said second port and said common area.

18. (Currently Amended) An integrated circuit according to claim 17 wherein said alignment means comprises a wiring trace and a signal buffering circuitry.

19. (Canceled)

20. (Currently Amended) An integrated circuit according to claim 19 17 wherein said first port and said second port are located at a substantial distance to each other relative to overall integrated circuit real estate.

21. (Currently Amended) A buffering circuitry with aligning ports that share a common area of integrated circuit real estate, said buffering circuitry comprising:

 a first area arranged on a wiring level of said integrated circuit real estate, said first area includes a set of output ports;

 a common area that is arranged in multilevel of said integrated circuit real estate, said common area includes signal buffering blocks provided on a semiconductor level, said common area also includes a first set and a second set of wiring traces provided in said wiring level, said common area is arranged so-as to allow for placement of said first and second sets of wiring traces to be within said common area, wherein said set of output ports of said first area is directly and

electrically connected to said first set of wiring traces of said signal buffering blocks without the use of a first linking area that includes bridge traces for linking mis-aligned ports with said first port and said common area; and

a second area arranged on said wiring level of said integrated circuit real estate, said second area includes a set of input ports that is electrically connected to said second set of wiring traces of said signal buffering blocks without the use of a second linking area that includes bridge traces for linking mis-aligned ports with said second port and said common area.